IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-23 (Canceled)

24. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a pair of first impurity regions being formed in the semiconductor substrate;

an active region formed between the pair of first impurity regions in the semiconductor substrate;

at least two second impurity regions formed in [[said]] the semiconductor substrate between the pair of first impurity regions;

at least one channel region between the at least two second impurity regions;

boundaries between the channel region and the at least two second impurity regions extending in a direction along a carrier flow direction of the channel region;

a floating gate formed over and insulated from the active region; and

a control gate formed over and insulated from the floating gate,

wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions, and

wherein a length of the second impurity regions is longer than a channel length in a channel length direction.

25. (Previously presented) A semiconductor device according to claim 24, wherein the at least two second impurity regions have a striped shape.

26-27. (Canceled)

28. (Previously presented) A semiconductor device according to claim 24, wherein an electronic device mounting the semiconductor device is any one of a mobile computer, a head-mounted display, a video camera, a cellular phone, a digital camera, a rear type projector, a front type projector.

29. (Currently Amended) A semiconductor device comprising:

a NOR type circuit having a plurality of memory transistors, the memory transistor comprising:

a semiconductor substrate;

a pair of first impurity regions being formed in the semiconductor substrate;

an active region formed between the pair of first impurity regions in the semiconductor substrate;

at least two second impurity regions formed in [[said]] the semiconductor substrate between the pair of first impurity regions;

at least one channel region between the at least two second impurity regions;

boundaries between the channel region and the at least two second impurity regions extending in a direction along a carrier flow direction of the channel region;

a floating gate formed over and insulated from the active region; and

a control gate formed over and insulated from the floating gate,

wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions, and

wherein a length of the second impurity regions is longer than a channel length in a channel length direction.

30. (Previously presented) A semiconductor device according to claim 29, wherein the at least two second impurity regions have a striped shape.

31-32. (Canceled)

33. (Previously presented) A semiconductor device according to claim 29, wherein an electronic device mounting the semiconductor device is any one of a mobile computer, a head-mounted display, a video camera, a cellular phone, a digital camera, a rear type projector, a front type projector.

34. (Currently Amended) A semiconductor device comprising:

a NAND type circuit having a plurality of one memory transistor, the memory transistor comprising:

a semiconductor substrate;

a pair of first impurity regions being formed in the semiconductor substrate;

an active region formed between the pair of first impurity regions in the semiconductor substrate;

at least two second impurity regions formed in [[said]] the semiconductor substrate between the pair of first impurity regions;

at least one channel region between the at least two second impurity regions;

boundaries between the channel region and the at least two second impurity regions extending in a direction along a carrier flow direction of the channel region;

a floating gate formed over and insulated from the active region; and

a control gate formed over and insulated from the floating gate,

wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions, and

wherein a length of the second impurity regions is longer than a channel length in a channel length direction.

35. (Previously presented) A semiconductor device according to claim 34, wherein the at least two second impurity regions have a striped shape.

36-37. (Canceled)

38. (Previously presented) A semiconductor device according to claim 34, wherein an electronic device mounting the semiconductor device is any one of a mobile computer, a head-mounted display, a video camera, a cellular phone, a digital camera, a rear type projector, a front type projector.

39. (Currently Amended) A semiconductor device comprising:

a semiconductor film;

a pair of first impurity regions being formed in the semiconductor film;

an active region formed between the pair of first impurity regions in the semiconductor film;

at least two second impurity regions formed in [[said]] the semiconductor film between the pair of first impurity regions;

at least one channel region between the at least two second impurity regions;

a floating gate formed over and insulated from the active region; and

a control gate formed over and insulated from the floating gate,

wherein the at least two second impurity regions have a dot-like shape or an elliptical shape, and

wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions.

40. (Canceled).

41. (Previously presented) A semiconductor device according to claim 39 further comprising a substrate, wherein the semiconductor film is formed over the substrate.

42. (Canceled).

43. (Previously presented) A semiconductor device according to claim 39, wherein an electronic device mounting the semiconductor device is any one of a mobile computer, a head-mounted display, a video camera, a cellular phone, a digital camera, a rear type projector, a front type projector.

44. (Currently Amended) A semiconductor device comprising:

a NOR type circuit having a plurality of memory transistors, the memory transistor comprising:

a semiconductor film;

a pair of first impurity regions being formed in the semiconductor film;

an active region formed between the pair of first impurity regions in the semiconductor film;

at least two second impurity regions formed in [[said]] the semiconductor film between the pair of first impurity regions;

at least one channel region between the at least two second impurity region;

a floating gate formed over and insulated from the active region; and

a control gate formed over and insulated from the floating gate,

wherein the at least two second impurity regions have a dot-like shape or an elliptical shape, and

wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions.

45. (Canceled).

46. (Previously Presented) A semiconductor device according to claim 44 further comprising a substrate, wherein the semiconductor film is formed over the substrate.

47. (Canceled).

48. (Previously presented) A semiconductor device according to claim 44, wherein an electronic device mounting the semiconductor device is any one of a mobile computer, a head-mounted display, a video camera, a cellular phone, a digital camera, a rear type projector, a front type projector.

49. (Currently Amended) A semiconductor device comprising:

a NAND type circuit having a plurality of one memory transistor, the memory transistor comprising:

a semiconductor film;

a pair of first impurity regions being formed in the semiconductor film;

an active region formed between the pair of first impurity regions in the semiconductor film;

at least two second impurity regions formed in [[said]] the semiconductor film between the pair of first impurity regions;

at least one channel region between the at least two second impurity regions;

a floating gate formed over and insulated from the active region; and

a control gate formed over and insulated from the floating gate,

wherein the at least two second impurity regions have a dot-like shape or an elliptical shape, and

wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions.

50. (Canceled).

51. (Previously presented) A semiconductor device according to claim 49 further comprising a substrate, wherein the semiconductor film is formed over the substrate.

52. (Canceled).

53. (Previously presented) A semiconductor device according to claim 49, wherein an electronic device mounting the semiconductor device is any one of a mobile computer, a head-

mounted display, a video camera, a cellular phone, a digital camera, a rear type projector, a front type projector.

54-56. (Canceled).

57. (Currently Amended) A semiconductor device according to claim 39 further ~~comprises~~ comprising an insulating layer that underlies the semiconductor film, wherein the insulating layer comprises the same conductivity type impurity element as the at least two second impurity regions.

58. (Currently Amended) A semiconductor device according to claim 44 further ~~comprises~~ comprising an insulating layer that underlies the semiconductor film, wherein the insulating layer comprises the same conductivity type impurity element as the at least two second impurity regions.

59. (Currently Amended) A semiconductor device according to claim 49 further ~~comprises~~ comprising an insulating layer that underlies the semiconductor film, wherein the insulating layer comprises the same conductivity type impurity element as the at least two second impurity regions.

60. (Previously presented) A semiconductor device comprising:

a semiconductor film including a source region, a channel forming region, and a drain region;

a pair of impurity regions formed at side edges along the channel length direction respectively;

a second impurity region formed between the pair of the impurity regions and along the channel length;

a floating gate formed over the channel forming region with a gate insulating film interposed therebetween; and

a control gate formed over the floating gate.

61. (Previously presented) A semiconductor device comprising:

a NOR type circuit including a memory transistor, the memory transistor comprising:

a semiconductor film including a source region, a channel forming region, and a drain region;

a pair of impurity regions formed at side edges along the channel length direction respectively;

a second impurity region formed between the pair of the impurity regions and along the channel length;

a floating gate formed over the channel forming region with a gate insulating film interposed therebetween; and

a control gate formed over the floating gate.

62. (Previously presented) A semiconductor device comprising:

a NAND type circuit including a memory transistor, the memory transistor comprising:

a semiconductor film including a source region, a channel forming region, and a drain region;

a pair of impurity regions formed at side edges along the channel length direction respectively;

a second impurity region formed between the pair of the impurity regions and along the channel length;

a floating gate formed over the channel forming region with a gate insulating film interposed therebetween; and

a control gate formed over the floating gate.

63. (Previously presented) A semiconductor device comprising:

a semiconductor film including a source region, a channel forming region, and a drain region;

a pair of impurity regions formed at side edges along the channel length direction respectively;

a field oxide film adjacent to the side edges;

a floating gate formed over the channel forming region; and

a control gate formed over the floating gate.

64. (Previously presented) A semiconductor device comprising:

a NOR type circuit including a memory transistor, the memory transistor comprising:

a semiconductor film including a source region, a channel forming region, and a drain region;

a pair of impurity regions formed at side edges along the channel length direction respectively;

a field oxide film adjacent to the side edges;

a floating gate formed over the channel forming region; and

a control gate formed over the floating gate.

65. (Previously presented) A semiconductor device comprising:

a NAND type circuit including a memory transistor, the memory transistor comprising:

a semiconductor film including a source region, a channel forming region, and a drain region;

a pair of impurity regions formed at side edges along the channel length direction respectively;

a field oxide film adjacent to the side edges;

a floating gate formed over the channel forming region; and

a control gate formed over the floating gate.

66-68. (Canceled)

69. (Previously presented) A semiconductor device according to claim 63, further comprising a second impurity region, wherein the second impurity region is formed between the pair of the impurity regions.

70. (Previously presented) A semiconductor device according to claim 64, further comprising a second impurity region, wherein the second impurity region is formed between the pair of the impurity regions.

71. (Previously presented) A semiconductor device according to claim 65, further comprising a second impurity region, wherein the second impurity region is formed between the pair of the impurity regions.

72. (Previously presented) A semiconductor device according to claim 60, wherein the pair of the impurity regions is opposite conductivity type of the source region and drain region.

73. (Previously presented) A semiconductor device according to claim 61, wherein the pair of the impurity regions is opposite conductivity type of the source region and drain region.

74. (Previously presented) A semiconductor device according to claim 62, wherein the pair of the impurity regions is opposite conductivity type of the source region and drain region.

75. (Previously presented) A semiconductor device according to claim 63, wherein the pair of the impurity regions is opposite conductivity type of the source region and drain region.

76. (Previously presented) A semiconductor device according to claim 64, wherein the pair of the impurity regions is opposite conductivity type of the source region and drain region.

77. (Previously presented) A semiconductor device according to claim 65, wherein the pair of the impurity regions is opposite conductivity type of the source region and drain region.

78. (Previously presented) A semiconductor device according to claim 60, wherein the semiconductor film is a single crystal silicon film or a polysilicon film.

79. (Previously presented) A semiconductor device according to claim 61, wherein the semiconductor film is a single crystal silicon film or a polysilicon film.

80. (Previously presented) A semiconductor device according to claim 62, wherein the semiconductor film is a single crystal silicon film or a polysilicon film.

81. (Previously presented) A semiconductor device according to claim 63, wherein the semiconductor film is a single crystal silicon film or a polysilicon film.

82. (Previously presented) A semiconductor device according to claim 64, wherein the semiconductor film is a single crystal silicon film or a polysilicon film.

83. (Previously presented) A semiconductor device according to claim 65, wherein the semiconductor film is a single crystal silicon film or a polysilicon film.

84. (Previously presented) A semiconductor device comprising:

an oxide film;

a crystalline semiconductor film formed on the oxide film, including a source region, a channel forming region, and a drain region;

three impurity regions formed along the channel length direction respectively;

a floating gate formed over the channel forming region with a gate insulating film interposed therebetween; and

a control gate formed over the floating gate,

wherein the oxide film is doped with an impurity having the same conductivity type as that of the three impurity regions.

85. (Canceled)

86. (Previously Presented) A semiconductor device according to claim 84, wherein three impurity regions are opposite conductivity type of the source region and drain region.

87. (Previously presented) A semiconductor device according to claim 84, wherein the semiconductor film is a single crystal silicon film or a polysilicon film.

88. (Previously Presented) A semiconductor device according to claim 24, wherein an impurity element concentration of the second impurity regions is in a range of 1×10^{17} to 5×10^{20} atoms/cm^3.

89. (Previously Presented) A semiconductor device according to claim 29, wherein an impurity element concentration of the second impurity regions is in a range of 1×10^{17} to 5×10^{20} atoms/cm^3.

90. (Previously Presented) A semiconductor device according to claim 34, wherein an impurity element concentration of the second impurity regions is in a range of 1×10^{17} to 5×10^{20} atoms/cm^3.